PATENTS
Attorney Docket No. 019705-000100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: D. Ton
Bulent Dervisoglu et al.	Art Unit: 2133
Application No.: 09/275,726	
Filed: March 24, 1999	EXPEDITED APPEAL UNDER MPEP §708.01(B)
For: ON-CHIP SERVICE PROCESSOR FOR TEST AND DEBUG OF INTEGRATED CIRCUITS	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The applicants of the patent application entitled above respectfully appeal the final Office Action of October 31, 2001 in which all pending claims 1-22 were rejected. The applicants appeal the rejection of all claims with the accompanying Appeal Brief in triplicate.

In accordance with MPEP §708.01(B), consideration of this appeal is expedited. The applicants filed a Petition to Make Special pursuant to 37 CFR §1.102 and MPEP §708.02 on August 22, 2000; upon which petition was granted on October 26, 2000 (Paper No. 6).

In addition to the brief filing fee according to 37 CFR §1.17(c), the applicants also submit herewith a fee for filing an extended response within the second month. The applicants filed a Notice of Appeal with a Certificate of Mailing, dated January 23, 2002 and received an acknowledgment of receipt of the Notice of Appeal, dated February 27, 2002. Rather than assume that the applicants' two-month period for filing an appeal brief pursuant to37 CFR §1.192(a) starts from the later date, the applicants submit the two-month late filing fee, under perhaps an overabundance of caution..

Respectfully submitted,

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Assistant Commissioner for Patents
Washington, D.C. 20231

On April 24, 2002
By: Gary T. Aka
Gary T. Aka

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Art Unit: 2133

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Real Party in Interest

The real party in interest is On-Chip Technologies, Inc., the assignee of the present patent application and wholly owned corporation of the applicant/inventors.

Related Appeals and Interferences

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

All claims 1-22 are pending; all claims 1-22 are appealed.

Status of Amendments

No amendments have been filed subsequent to the final rejection of all claims 1-22 in the Office Action of October 31, 2001.

Summary of Invention

The present invention is related to the testing and debugging of integrated circuits. Generally stated, there are two ways of testing and debugging integrated circuits, both of which are described in the applicants' specification. One way is to serially "scan" in test vectors, sets of predetermined bits into predetermined locations in the integrated circuit, operate the integrated circuit and to scan out the test results from locations in the integrated circuit. See applicants' specification, page 2, lines 4-33. The other way is to "probe" the integrated circuit, that is, to observe the internal workings of the integrated circuit in its normal operation. See, for example, applicants' specification, page 3, lines 1-15. The applicants' invention, as reflected by the pending claims under appeal, is directed toward the latter probing technique.

One aspect of the present invention is related to the operation of the integrated circuit and reflected in independent method claim 15. The following steps are used: operating logic blocks of the integrated circuit to perform normal system operations at the integrated circuit's normal clock rates to produce sets of system operation signals, i.e., the normal system operation signals; enabling probe lines in the integrated circuit to capture and carry the sets of the system operation signals of the logic blocks at the normal clock rates; retrieving the sets of system operation signals from the logic blocks along the probe lines at the normal clock rates, storing the sets of the system operation signals in a memory in the integrated circuit at the normal clock rates; and processing the sets of stored system operation signals to perform test and debug operations of the logic blocks of the integrated circuit. The applicants' specification at page 19, lines 8-21, has a description of such probe testing with an external diagnostic console.

The device aspect of the present invention is reflected in independent claims 1 and 10. In one aspect of the applicants' invention, the integrated circuit has a control unit, a memory and a plurality of probe lines. The control unit performs test and debug operations of the logic blocks of the integrated circuit. The memory which is associated with the control unit, holds instructions for the control unit and captures system operation signals. The probe lines which are responsive to the control unit, carry system operation signals from predetermined probe points of the logic blocks to the memory for storage. The probe lines comprise strings of storage elements which provide the signal paths from the probe points to

the memory to move sets of the system operation signals at system operation clock rates. See applicants' specification, page 7, lines 9-21; page 17, lines 9-27; Fig. 11. In other words, the internal clock(s) of the integrated circuit are used to move the system operation signals at high speed into the memory. The sets of system operation signals are stored in the memory for subsequent retrieval and analysis. See applicants' specification, page 6, lines 20-30.

Another device aspect of the invention is that the integrated circuit has an interface for coupling to an external diagnostic processor. Applicants' specification, page 16, lines 15-20; page 17, lines21-22; Fig. 1b. The control unit is responsive to instructions from the external diagnostic processor to capture sets of sequential system operation signals of the integrated circuit through the probe lines into the memory. The memory is coupled to the control unit and the interface so that the stored sets of sequential system operation signals are retrieved from the memory through the interface to the external process at one or more clock signal rates external to the integrated circuit so that the external diagnostics processor can process the captured system operation signals for analysis. See page 19, lines 8-21.

Issues

Only one basic issue is appealed, that is, whether the Examiner has made a proper case of obviousness in rejecting the applicants' invention as recited in independent claims 1, 10 and 15. The applicants argue below that the Examiner has not even met the criteria for a *prima facie* case in rejecting the basic aspects of their invention, as recited in independent claims 1, 10 and 15. These base claims are allowable and since the independent claims are allowable, all remaining claims 2-9, 11-14, and 16-22 are allowable. That is, all pending claims 1-22 should be allowed and passed to issue.

Grouping of Claims

Claims 1-10 and 13-22 were rejected for obviousness by the combination of the Rajski and Gheewala '090 patents, US. Patent Nos. 5,991,898 and 5,065,090 respectively. The claims of this group do not stand nor fall together, rather independent claims 1, 10 and 15 are separately patentable, as pointed out in the Argument section below.

Dependent claims 11-14 were also rejected for obviousness by the combination of the Rajski and Gheewala '090 patents, and a second Gheewala patent, U.S. Patent No.

5,202,624. The applicants do not select a representative claim for this group since the rejection of the previous claim grouping presents more significant issues for appeal.

Argument

Applicants' independent claims 1, 10 and 15 were rejected under 35 U.S.C. §103(a) for obviousness over U.S. Patent No. 5,991,898, which issued November 23, 1999 to J. Rajski *et al.* (hereinafter the "Rajski patent"), in view of U.S. Patent No. 5,065,090 which issued November 12, 1991 to T. Gheewala *et al.* (hereinafter the "Gheewala '090 patent"). In rationalizing his rejection, the Examiner stated:

> "Rajski teaches the invention as substantially as claimed including an integrated circuit [INTEGRATED CIRCUIT 10, Fig. 1] having logic blocks [CUT 14, Fig. 1] comprising:
>
> "a control unit [embedded processor core 12, Fig.1] for performing test and debug operations of said logic blocks of said integrated circuit;
>
> "a memory [non-volatile memory 18, Fig. 1] associated with said control unit, said memory holding instructions for said control unit [col. 5 lines 50-60].
>
> "Rajski does not teach a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points wherein said probe lines comprises strings of storage elements providing signals paths from said probe point.
>
> "Gheewala teaches a cross-check test structure consists of serial/ parallel shift registers with probe lines and sense lines to control the probe lines and to observe the output of the sense lines (Fig. 4 and col. 8 lines 21-56).
>
> "It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test of multiple scan based integrated [circuit (sic)] to have a test structure consists of shift registers with probe lines for controlling and observing the probe lines as taught by Gheewala. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would reduce the external probe points

requirement to less than 10 compare to 200 probe points [see Gheewala col. 3 lines 66 – col. 4 lines 4]."

In contrast to the applicants' claimed invention by which probe lines are used to extract data from the internal workings of an integrated circuit in normal operation, both of the cited references use serial scanning techniques to test the integrity of an integrated circuit. To perform such scan testing, the integrated circuit is placed in a test operation (in contrast to a normal operation) mode, and test pattern signals, sometimes termed a test vector, are scanned into the integrated circuit at selected locations in the integrated circuit into known states. The resulting test response data, sometimes termed test results, are scanned out for analysis.

The Rajski patent uses BIST (Built-In Self Test) techniques to generate the scanned-in test patterns and to compact the scanned-out test results. Rajski specification, col. 1, lines 29-32. With the assumption that the integrated circuit has embedded cores and high-performance computing system elements, such as DSP (Digital Signal Processing) circuits, micro-controllers, and microprocessors, the Rajski patent describes the use of these processing elements to also perform the testing of the integrated circuit, rather than append special test circuits for the BIST. To the mission microcode which instructs the processing elements (termed "embedded processor core" in the body of the Rajski patent; see col. 3, line 66, for example) in their system operations is added BIST microcode to generate the test vectors and to compact the results. See col. 3, lines 27-51. The particular teaching of the Rajski patent is the further testing of circuits peripheral to the embedded processor core, termed peripheral devices and labeled CUTs (Circuits Under Test) 14, with this form of BIST. See, e.g., col. 3, lines 54-62 and col. 4, lines 32-38; Fig. 1.

The Gheewala '090 patent describes an integrated circuit with a grid test structure with intersecting probe lines P1-PN (carrying control signals) and sense lines S1-SM (carrying signals to or from the integrated circuit sense points). At each intersection, an electronic switch responsive to a signal on a probe line controls the connection of the sense point to a sense line. A shift register 27 is connected to the probe lines P1-PN and a second shift register 28 is connected to the sense lines S1-SM to provide on-chip test electronics to

reduce the number of probe points, i.e., test pins, for the integrated circuit. See, for example, the Abstract of the Gheewala '090 patent; Fig. 4 and col. 8, lines 21-56 of the specification.

Neither of these references, singly or in combination, teaches nor even hints at the applicants' claimed invention. This combination of references fails to make even a *prima facie* case of obviousness. MPEP §2143 states,

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

The applicants illustrate below the Examiner's failure to make a *prima facie* case of obviousness with respect to method claim 15 first, then device claims 1 and 10. This arrangement of arguments better explains the differences between the applicants' claimed invention, but also points out the additional separately patentable features of the independent claims. For example, all the claims are concerned with the testing of an integrated circuit with normal system operation signals, in contrast with special test result signals of the cited patent references. Besides claiming an integrated circuit device in contrast to the method claim 15, claim 1 recites a limitation of the retrieval of system operation signals from memory. Claim 10 further has the limitations that the system operation signals are sequential and there are different clock rates for storing system operation signals into memory and retrieving the signals from memory.

I. A *Prima Facie* Case of Obviousness for Rejecting Representative Claim 15 Has Not Been Made.

Claim 15 recites:

> "A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising
>
> operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit."

As rationalized by the Examiner, the Rajski patent teaches all the elements of the applicants' claim, except for the recited probe lines which are purportedly taught by the Gheewala '090 patent. A reading of the cited references shows that a) neither of the references deal with the applicants' "system operation signals"; b) neither of the references teach operations "at system clock signal rates"; c) the Rajski patent does not teach the applicants' "memory"; and d) there exists no motivation to combine the two cited references.

A. In Contrast to the Applicants' Claim, the Cited References Do Not Deal with "System Operation Signals".

As described above, the applicants' invention is concerned with the operation of an integrated circuit in its normal operation state. See, for example, the applicants' specification, page 3, lines 3-6; page 7, lines 9-23; page 19, lines 14-15. Likewise, claim 15 explicitly recites the step of "operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals" and performing the other steps recited in the claim.

On the other hand, the cited references are both concerned with test mode signals. The Rajski patent describes the start of its operations at col. 6, lines 44-46. "As shown, for the illustrated embodiment, in step 21, embedded processor 12 is first placed in test mode." Then the subsequent testing procedures are described. Hence the subject integrated circuit is not in "normal system operations" mode and, by definition, there can be no "system operation signals," as called for in applicants' claim 15. Furthermore, the Examiner adds the teachings of the Gheewala '090 patent to the Rajski patent to match the applicants' "probe lines". Even assuming *arguendo* that the Gheewala teachings are truly analogous to the applicants' "probe lines," the combined system does not handle "system

operation signals," as claim 15 requires, since the Rajski components necessarily operate in test mode.

Finally, the Gheewala '090 patent itself teaches a test mode for operating the sense lines S1-SM, which the Examiner has analogized to the applicants' probe lines. Gheewala states at col. 8, line 66 – col. 9. line 2, "In the normal operating mode for the Integrated Circuit, all the probe-lines P1 through PN are maintained in the deselect mode, so that the sense-lines are disconnected from the test-points that are monitored during test." In other words, during normal operation of the subject integrated circuit, the probe lines P1-PN which act as control lines for the sense lines S1-SM (the Examiner's purported probe lines), render the sense lines S1-SM inoperative. The sense lines S1-SM cannot carry "system operation signals" during the normal operating mode of the integrated circuit.

Hence neither of the cited patents teaches the handling of "system operation signals," as recited in claim 15.

B. The Cited References Do Not Teach Operations of the Integrated Circuit "at System Clock Signal Rates."

Related to the argument that the two cited references do not teach the handling of "system operation signals," claim 15 recites the operation of the integrated circuit "at system clock signal rates internal to said integrated circuit." The system clock signal rates are applicable to the steps of "operating said logic blocks..."; "enabling said probe lines..."; "retrieving said sets of system operation signals..."; and storing "said sets of system operation signals...".

As noted above, both the Rajski patent and the Gheewala '090 patent operate in a test mode during test operations. Hence, by definition, neither reference has an integrated circuit carrying out the steps recited in claim 15 at "system clock signal rates internal to said integrated circuit to produce sets of system operation signals."

C. The Memory of the Rajski Patent Cannot "Store System Operation Signals".

The Examiner relies upon the Rajski patent for a memory which stores system operation signals, as called for in applicants' claim. However, the memory 18 is described as being nonvolatile. E.g., see the Rajski patent, col. 5, line 32. Such a memory cannot be used

for storing sets of system operation signals as called for in the claim 15, i.e., "...storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit...". Once manufactured, a nonvolatile memory either cannot be written into, e.g., a ROM (Read-Only Memory), or may be written into only under special conditions, i.e., with special (high) programming voltages and special (long) programming times, such as EEPROM (Electrically Eraseable Programmable Read-Only Memory). This is well known to persons familiar with semiconductors and computer systems. Typically, non-volatile memory is used to store program code or data which must be preserved even after power is shut off; non-volatile memory is not usable in operations which require in-situ and frequent Write operations. This is consistent with the Rajski patent which describes that the memory 18 holds the instructions that are to be executed by the embedded processor core 12. In Fig. 1, the arrow between the embedded processor core 12 and non-volatile memory 18 points in only one direction, from the memory 18 toward the processor core 12, contrary to the storage of sets of system operation signals in the non-volatile memory 18.

Furthermore, claim 15 specifically requires that the sets of system operation signals be stored at "system clock signal rates...". Even assuming that the non-volatile memory 18 did store system operation signals, it could not so at such high speed. As pointed out above, non-volatile memories require special programming voltages and special programming times.

For the sake of completeness, the applicants note that the Rajski patent also briefly describes the memory 18 in terms of volatile memory. See col. 6, lines 38-42. However, the description of an alternative storage memory medium is mentioned in passing and for the same purpose as the nonvolatile memory, the storage of the ABIST microcode for the embedded microprocessor core 12. There is no description nor even a hint of the storage of anything other than microcode, far different from the applicants' language, "system operation signals in said memory at said system clock signal rates internal to said integrated circuit."

D. There is No Suggestion nor Motivation to Combine the Gheewala '090 Patent With the Rajski Patent.

To make up for the lack of the applicants' probe lines in the Rajski patent, the Examiner added the sense lines S1-SM in the Gheewala '090 patent. The Examiner reasoned,

"It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test of multiple scan based integrated [circuit (sic)] to have a test structure consists of shift registers with probe lines for controlling and observing the probe lines as taught by Gheewala. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would reduce the external probe points requirement to less than 10 compare to 200 probe points...."

This combination with the Gheewala '090 patent with the Rajski patent is artificial and forced. Both references teach serial scan techniques. Why one skilled in the art would create an integrated circuit with two serial scan architectures is not explained and the advantages of such a combination does not make sense. The Rajski patent already teaches the reduction of the external probe points, i.e., test pins for the integrated circuit, by using Built-In Self Test (BIST) technology. In placing a context for their described improvements in BIST, Rajski *et al.* state, "Practical importance of this problem (testing of integrated circuits) in conjunction with the increasing complexity of VLSI circuits not balanced by a corresponding increase in the number of input and output pins, has made built-in self test (BIST) one of the most important technology in IC testing that is expected to profoundly influence the area requirement of ICs in upcoming years." Col. 1, lines 22-28.

The Gheewala '090 patent, on the other hand, teaches a two-dimensional array test structure for integrated circuits. Each intersection of probe and sense lines defines a test point so that, in the example given by Gheewala, a 100x100 test array has 10,000 test points and 200 test lines, probe and sense. To reduce the 200 test pins, termed "probe-points," connected to the test lines, the Gheewala '090 patent also teaches connecting serial/parallel shift registers to the test lines. Hence the number of probe-points from 200 to less than 10. See Gheewala '090 patent, col. 3, line 60 – col. 4, line 4. Nonetheless, this test solution results in 200 clock cycles for each set of 200 test lines to clock in control signals and test result signals out (see Fig. 4 and col. 8, lines 21-56, portions which were cited by the Examiner), which result in a slowing of test operations. In other words, Rajski *et al.* believe that BIST technology solves the testing problem for integrated circuits of increasing complexity and lack of corresponding increase in test pins. Gheewala would require more test

pins, albeit with a reduced number of test pins, but at the cost of longer testing times. Hence why anyone would be motivated to create an integrated circuit built in accordance with the teachings of the Rajski patent and then add a second scan-based testing circuits of the Gheewala '090 patent is not clear and unexplained.

II. A *Prima Facie* Case of Obviousness for Rejecting Representative Claim 1 Has Not Been Made.

The rejection of device claim 1 for obviousness is likewise unsupportable. Applicants' claim 1 calls for:

> "An integrated circuit having logic blocks comprising
> a control unit for performing test and debug operations of said logic blocks of said integrated circuit;
> a memory associated with said control unit, said memory holding instructions for said control unit; and
> a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable."

The same arguments for the lack of a *prima facie* case with respect to method claim 15 are also applicable to claim 1 and even further arguments can be made.

A. The Previous Arguments With Respect to Claim 15 are Applicable to the Rejection of Claim 1.

Claim 1 calls for "...system operation signals from predetermined probe points...". As argued above, neither the Rajski patent nor the Gheewala '090 patent deal with system operation signals, as called for by the applicants' claim.

Claim 1 also requires probe lines which are "capable of carrying sets of said system operation signals at system operation clock rates...". As noted above, neither the Rajski patent nor the Gheewala '090 patent operate in the normal operation mode to carry out their serial scan test result signals. As such, the Examiner's purported probe lines, i.e., the sense lines S1-SM of Gheewala '090 patent do not operate as system operation clock rates.

Claim 1 also requires the storage of the system operation signals into memory, "said sets of system operation signals stored in said memory...". As argued above, the

nonvolatile memory 18 of the Rajski patent does not provide a memory which can store system operation signals, as claimed by the applicants.

The rejection of claim 1 also requires the combination of the Rajski and Gheewala '090 patents, according to the Examiner. As pointed above, there is no motivation to combined these two serial-scan testing patents.

Finally, claim 1 also has additional grounds for arguing that a *prima facie* case has not been made.

B. The Rajski Patent Does Not Teach the "Retrieval of System Operation Signals" from Memory.

The end of claim 1 recites, "...said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable." This language cannot be met by the combination of references cited by the Examiner.

Even assuming *arguendo* that the scan test responses are "system operation signals," and the test responses are stored in the non-volatile memory 18 of the Rajski patent, these putative system operation signals are not retrievable from memory. The Rajski patent describes compacting the test responses in a cascaded add-and-accumulate manner to reduce the impact on an error compensation phenomenon. See col. 4, lines 23-31. A well-known aspect of all signature compaction techniques is that it is impossible to reverse the process to obtain the original uncompacted input data from the final compacted signature. Rajski's computed output signature is used to determine if the received input sequence is the same as the predetermined sequence on which the output signature had been pre-computed. If the final signature is different from the pre-computed final signature, the only conclusion which can be drawn is that the input sequence is different from the expected input sequence upon which the expected signature had been pre-computed. The actual input sequence cannot be identified, as is well-known to test design engineers. This is the nature of the compaction techniques cited in the Rajski specification, col. 14, line 46 – col. 15, line 12.

Hence, the system operation signals cannot be retrieved.

III. A *Prima Facie* Case of Obviousness in Rejecting Representative Claim 10 Has Not Been Made.

Applicants' claim 10 calls for:

> "An integrated circuit comprising
> an interface for coupling to an external diagnostic processor;
> a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;
> a plurality of probe lines coupled to said unit for carrying said system operation signals from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;
> a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals."

From the similarity of the language of claim 10 to that of claim 1 (and 15), previous arguments are also applicable to claim 10. The language of claim 10 also provides additional arguments that a *prima facie* case of obviousness has not been made.

A. All the Previous Arguments are Applicable to the Rejection of Claim 10

The same arguments with respect to claim 1 are applicable to claim 10. That is, a) neither the Rajski patent nor the Gheewala '090 patent deals with "system operation signals," as called for in the unit, probe lines and memory elements of claim 10; b) neither of the cited references teach moving sets of system operation signals along probe lines and storing sets of system operation signals into memory "at system operation clock rates"; c) the memory of the Rajski patent cannot store system operation signals; b) the Rajski Patent does not teach the storage of sets of system operation signals into memory; c) the Rajski Patent does not teach the retrieval of sets of system operation signals from memory; d) there exists no motivation to combine the Rajski patent with the Gheewala '090 patent; and e) the Rajski patent does not teach the retrieval of system operations signals from memory, as recited in claim 10.

Claim 10 also recites that the system operation signals are sequential, i.e., "sets of sequential system operation signals," and that there are differential speeds in storing and

retrieving system operation signals. This provides additional arguments why a *prima facie* case of obviousness has not been made by the Examiner.

B. The Gheewala '090 Patent Does Not Teach Probe Lines Which Move Sets of "Sequential" System Operation Signals.

Claim 10 recites in particular, "...said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates...."

The Examiner asserts that Fig. 4 and col. 8, lines 21-56, of the Gheewala '090 patent describes the probe lines claimed by the applicants, but not taught by the Rajski patent. The language of claim 10 is simply not met by an examination of Fig. 4 and a perusal of the cited sections of the Gheewala '090 patent. After capturing the signals on the sense lines S1-SM, which the Examiner has analogized to the applicants' probe lines, in the shift register 28, which the Examiner has analogized to the applicants' strings of storage elements, in parallel, the captured signals in the shift register 28 are read out. "Next, the signals stored in the shift-register 28 can be serially read out at probe-point 32 for analysis by external test electronics. This is achieved by applying an external signal to the parallel/serial control probe-point 29 to put the shift-register 28 in a serial mode and turning the clock 30 ON and OFF M times." Col. 8, lines 40-45.

In contrast, claim 10 calls for the movement of "sets of sequential system operation signals at system operation clock rates." Even if, assuming *arguendo* that, the shift-register 28 were running at system operation clock rates, the highest clock rates possible in an integrated circuit, the shift-register 28 could not capture the next set of sequential system operation signals. Rather the shift-register 28 would capture system operation signals every M system clock cycles. This would allow the M bits stored in the shift-register 28 to be shifted out and the next set of system operation signals to be captured M system clock cycles later. Hence even assuming *arguendo* the combination of the Gheewala '090 patent with the Rajski patent, the limitations of claim 10 cannot be met.

C. None of the Cited References Teach Differential Speeds for the Storage and Retrieval of System Operation Signals.

Finally, the applicants point out that claim 10 calls for "...sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to

said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit...(underline added)." Nowhere does the Examiner indicate in the Rajski and Gheewala '090 patents where such a differential clocking is performed. Again, the Examiner has failed to make a *prima facie* case of obviousness.

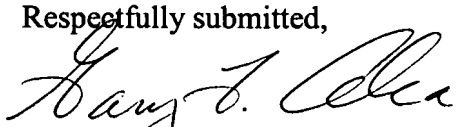
IV. Summary and Conclusion of Arguments

From the arguments above, it should be evident that the Examiner has not been met his burden of providing a *prima facie* case of obviousness to reject representative independent claims 1, 10 and 15. The requirements of MPEP §2143 have not been met. The Examiner has not provided nor pointed out, a credible motivation for combining the cited Rajski and Gheewala '090 patents. Even if made, the combination of the references to reach applicants' claimed invention. Finally, the references, either singly or in combination, neither teach nor even suggest all of the limitations in the applicants' claims.

Hence claims 1, 10 and 15 are unobvious over the cited Rajski and Gheewala '090 patents and should be allowed.

Therefore, the applicants respectfully request that the rejections be removed, all pending claims 1-22 be allowed, and the case passed to issue.

Respectfully submitted,



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Appendix

The following claims 1-22 as pending in this appeal. Representative independent claims 1, 10 and 15 argued in this appeal are marked in bold:

1. An integrated circuit having logic blocks comprising

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; and

a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable.

2. The integrated circuit of claim 1 further comprising

a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit.

3. The integrated circuit of claim 2 further comprising

a unit coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

4. The integrated circuit of claim 2 wherein said scan lines comprise a first string of flip-flop connectors connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode.

5. The integrated circuit of claim 2 wherein said scan lines comprise a second string of flip-flop connectors between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode.

6. The integrated circuit of claim 1 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode.

7. The integrated circuit of claim 6 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

8. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying digital state system operation signals.

9. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals reflective of analog conditions at said predetermined probe points.

10. An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

11. The integrated circuit of claim 10 wherein said unit further comprises trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory.

12. The integrated circuit of claim 11 wherein said trigger logic is responsive to said system operation signals for terminating storage of said set of said system operation signals in said memory.

13. The integrated circuit of claim 10 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points in one mode.

14. The integrated circuit of claim 13 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

15. A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

16. The method of claim 15 wherein said system operation signals comprise sequential system operation signals.

17. The method of claim 16 wherein said system operation signals comprise sets of sequential system operation signals.

18. The method of claim 15 wherein said integrated circuit has a plurality of scan lines of said logic blocks, said method further comprising

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving test signal results from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit,

storing said test signal results in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

19. The integrated circuit of claim 10 wherein said memory is also coupled to said system operation unit so that said memory unit may be accessed selectively or simultaneously by said data capture unit and said system operation unit.

20. The method of claim 1 wherein said system operation signals comprise sequential system operation signals.

21. The method of claim 20 wherein said system operation signals comprise sets of sequential system operation signals.

22. The method of claim 1 wherein said system operation signals are stored in said memory at one or more clock signal rates internal to said integrated circuit.